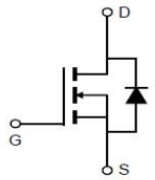
●General Description

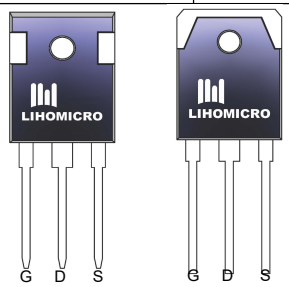
The N-Channel MOSFET LH40N50 has the low $R_{DS(on)}$,low gate charge,fast switching and excellent avalanche characteristics.This device is suitable for fast charge and lighting.



V DS =650V

$R_{DS(ON)}$=0.085Ω

I D =46A



TO-247 TO-3P

■ RoHS COMPLIANT

●Features

- ■Advanced Planar Process
- ■RDS(ON),typ.=85 mΩ@VGS=10V Low $R_{DS(on)}$ & FOM
- ■Low Gate Charge Minimize Switching Loss
- ■Rugged Poly silicon Gate Structure

●Application

- ■BLDC Motor Driver
- ■Electric Welder
- ■High Efficiency SMPS

●Ordering Information:

Part Number	LH40N50	LH40N50
Package	TO-247	TO-3P
Basic Ordering Unit (pcs)	1000	1000
Normal Package Material Ordering Code	LH40N50T2-TO247-TU	LH40N50T3-TO3P-TU
Halogen Free Ordering Code	LH40N50T2-TO247-TU-HF	LH40N50T3-TO3P-TU-HF

●Absolute Maximum Ratings（TC =25℃）

PARAMETER	SYMBOL	Value	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current ,T_C = 25°C	I_D	46	A
	I_D(T_C=100°C)	30	
Pulsed Drain Current at VGS=10V[2,4]	I_{DM}	180	A
Single Pulse Avalanche Energy	E_{AS}	5000	mJ
Peak Diode Recovery dv/dt[3]	dv/dt	5.0	V/ns
Power Dissipation	P_D	540	W
Derating Factor above 25℃		4.32	W/℃
Operating Temperature	T_J	-55~+150	℃
Storage Temperature	T_{STG}	-55~+150	℃
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L	300	℃
	T_{PAK}	260	

●Electronic Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D=250uA	500	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0	--	4.0	V
Drain-source On Resistance	$R_{DS(ON)}$	V_{GS} =10V, I_D=23A		85	100	mΩ
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V,V_{GS}=0V,T_J=25℃	--	--	5	uA
		V_{DS}=400V,V_{GS}=0V,T_J=125℃	--	--	500	
Gate-Source Leakage Current	I_{GSS}	$V_{GS=}$+30V,$V_{DS=}$0V	--	--	+100	nA
		$V_{GS=}$-30V,$V_{DS=}$0V	--	--	-100	
Forward Transconductance	g_{FS}	V_{GS} =25V, I_D=23A	--	32	--	S
Input Capacitance	Ciss	VGS=0V, VDS=25V, f=1MHz	--	1.0	--	nF
Output Capacitance	Coss		--	0.7	--	
Reverse Transfer Capacitance	Crss		--	0.1	--	
Turn -Off Delay Time	Td(off)	V_{GS}=10V, V_{DD}=250V, R_G=10Ω, ID=23A	--	100	--	ns
Fall time	tf		--	36	--	
Turn-on delay time	td(on)		--	25	--	
Rise time	tr		--	39	--	
Total Gate Charge(10V)	Qg	V_{GS}=0Vto 10V, V_{DS}=250V, ID=23A	--	138	--	nC
Gate-to-Source Charge	Qgs		--	38	--	
Gate-to-Drain Charge	Qgd		--	27	---	
Continuous Diode Forward Current[1,5]	I_S	Integral PN-diode in MOSFET	--	--	46	A
Pulsed Source Current[2]	I_{SM}		--	--	180	
Diode Forward Voltage[2]	V_{SD}	Is=46A,V_{GS} =0V	--	--	1.5	V
Reverse Recovery Time	trr	V_{GS}=0V, If=46A, di_F/dt=100A/μs	--	730	--	ns
Reverse Recovery Charge	Qrr		--	3.0	--	uC

●Thermal Characteristics

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance Junction-case	Rth_{JC}	0.23	℃/W
Thermal Resistance Junction-ambient	Rth_{JA}	50	℃/W

Notes:

1.T_J=+25℃to +150℃

2.Silicon limited current only.

3.Package limited current.

4. Repetitive rating,pulse width limited by maximum junction temperature.

5.Pulse width≤380uS; duty cycle≤2%.

●Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

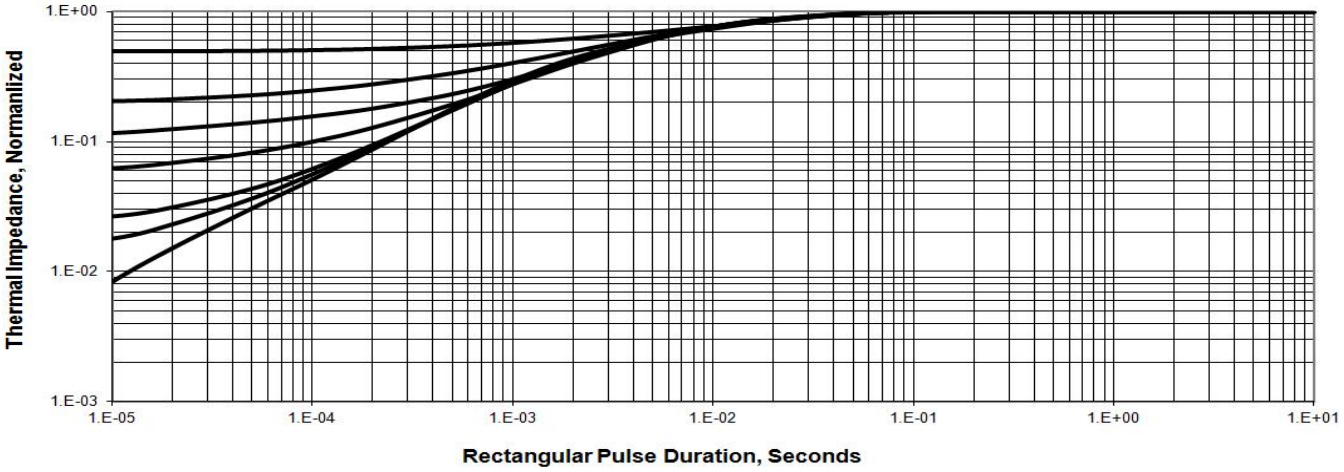


Figure 2 . Max. Power Dissipation vs Case Temperature

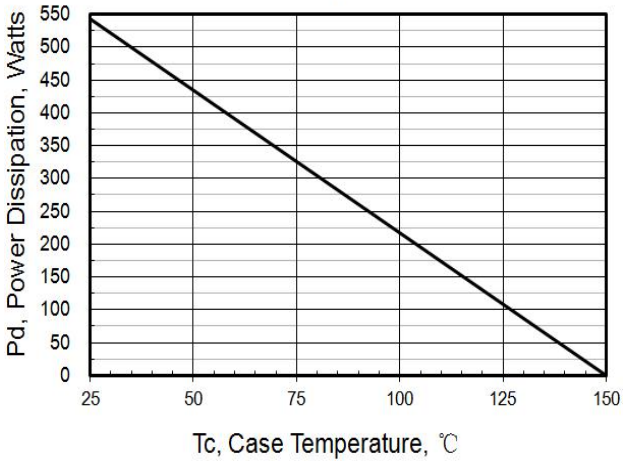


Figure 3 .Maximum Continuous Drain Current vs Tc

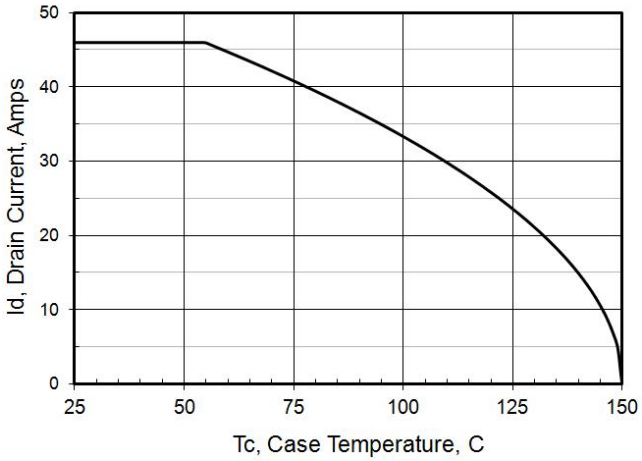


Figure 4. Typical Output Characteristics

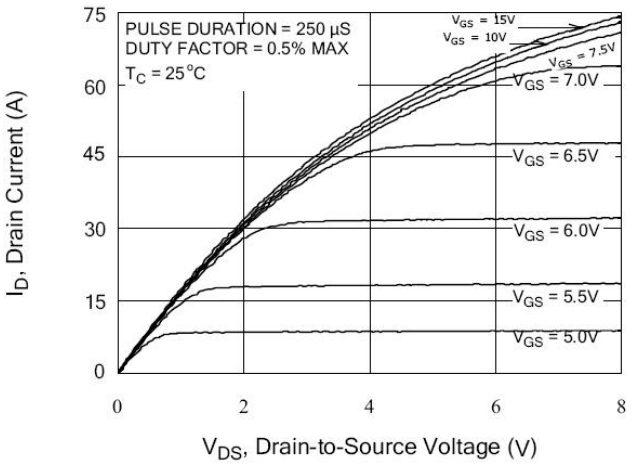
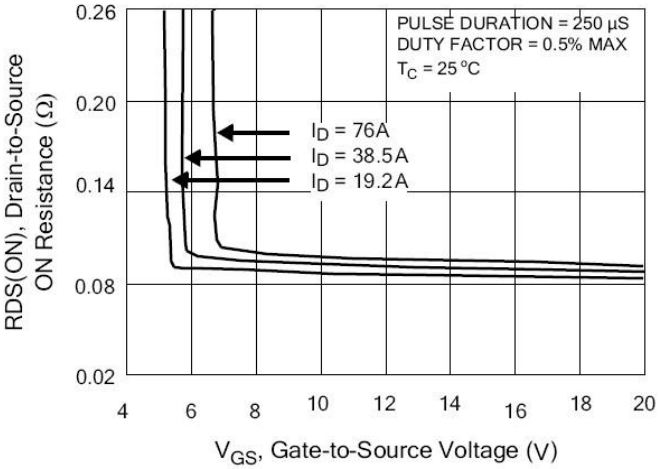


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



●Typical Characteristics(cont.)

Figure 6. Peak Current Capability

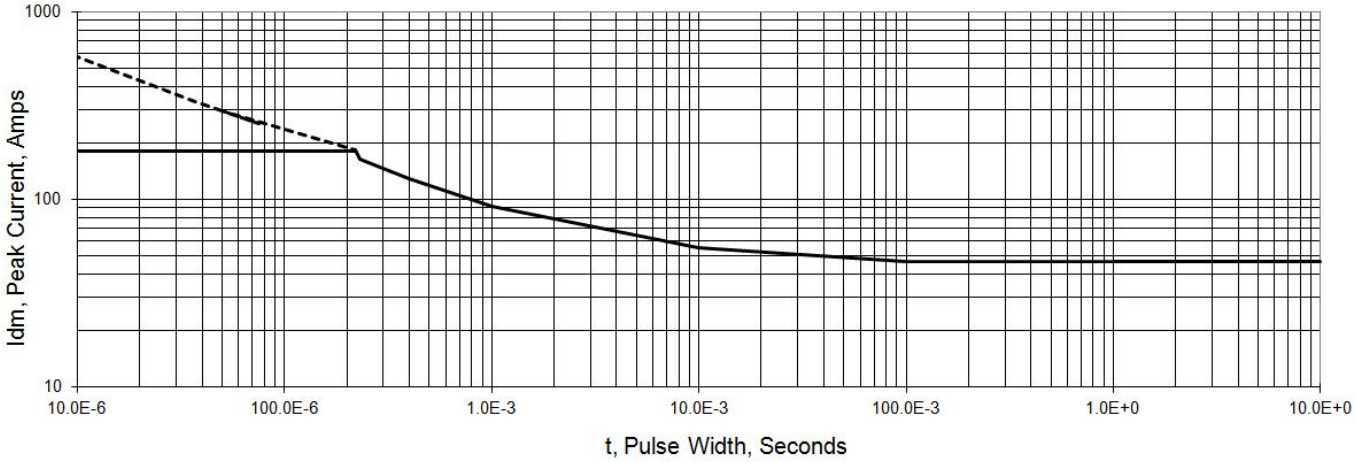


Figure 7. Typical Transfer Characteristics

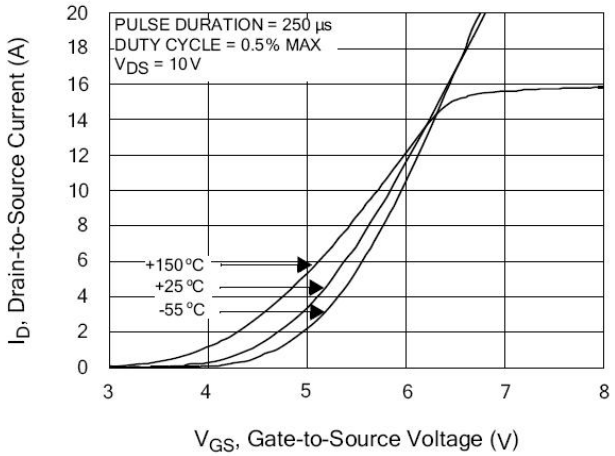


Figure8. Unclamped Inductive Switching Capability

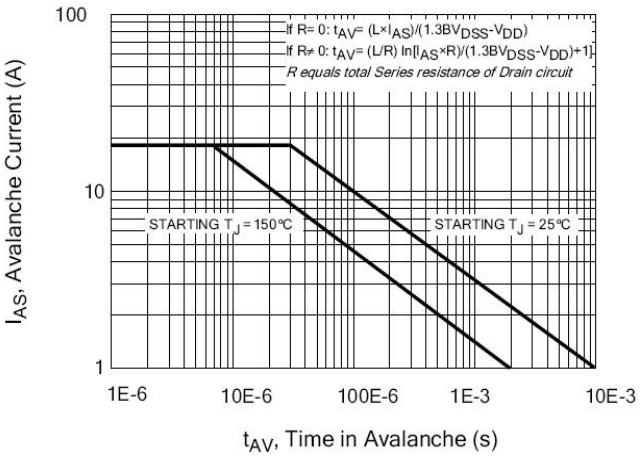


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

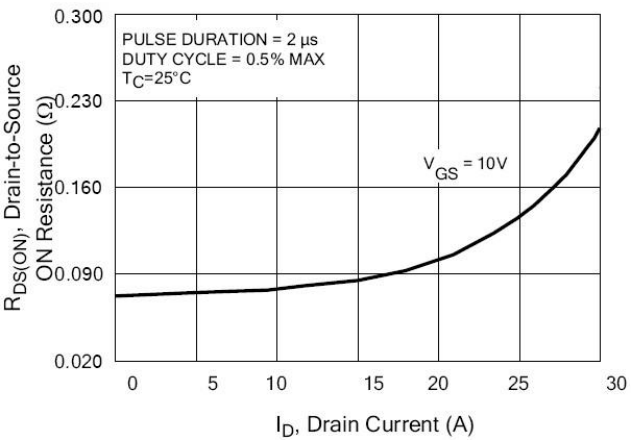
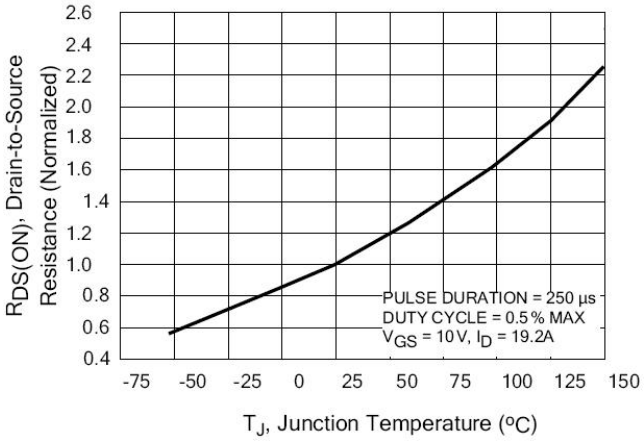


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



●Typical Characteristics(cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

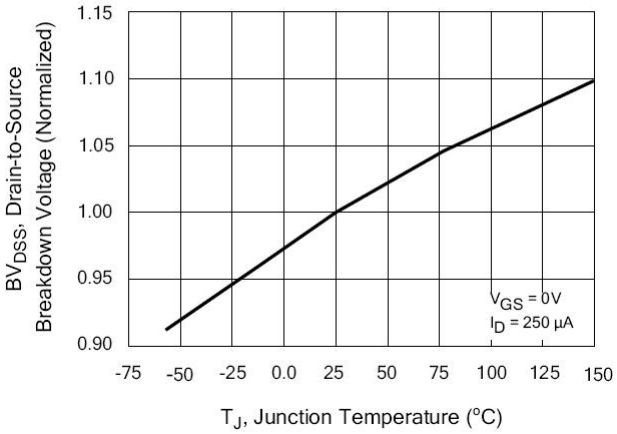


Figure 12. Typical Threshold Voltage vs Junction Temperature

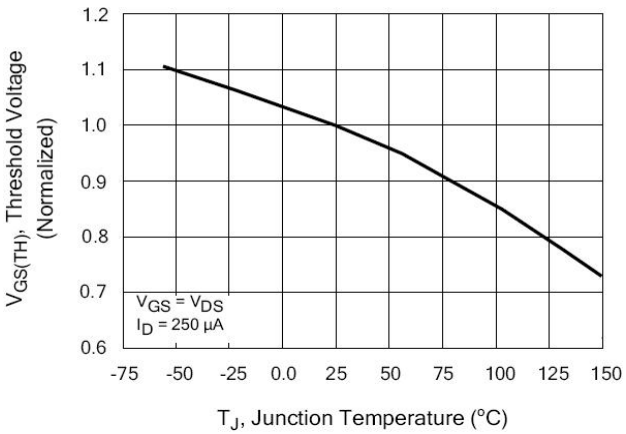


Figure 13. Maximum Forward Bias Safe Operating Area

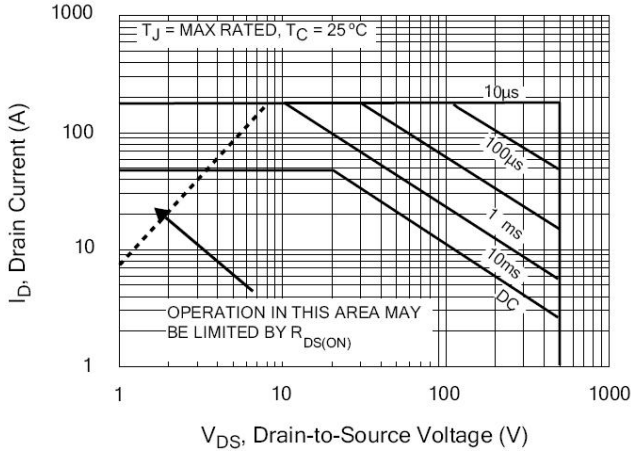


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

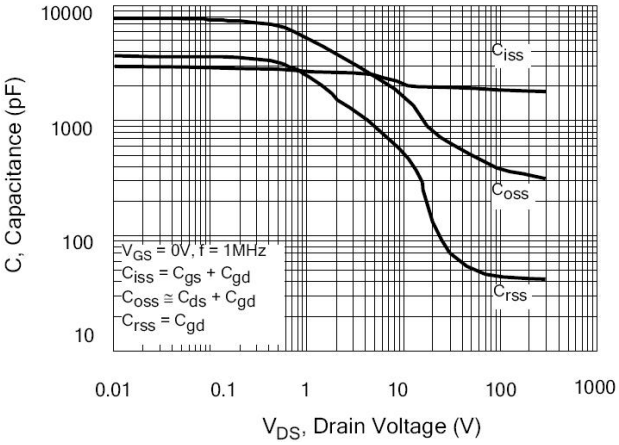


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

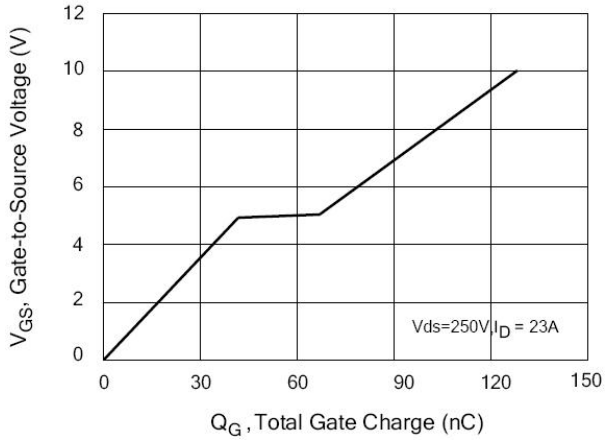
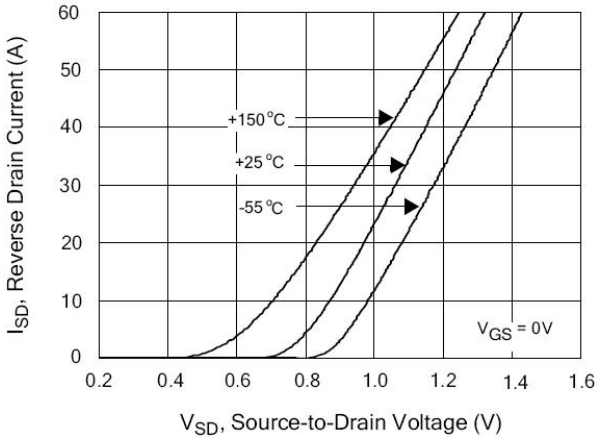


Figure 16. Typical Body Diode Transfer Characteristics



●Test Circuits & Waveforms

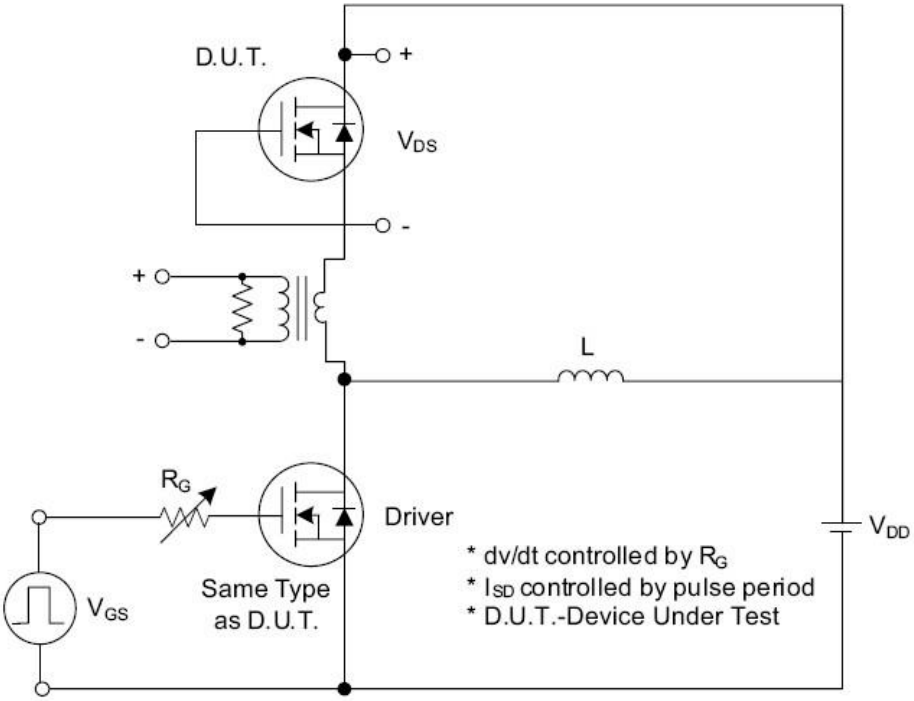


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

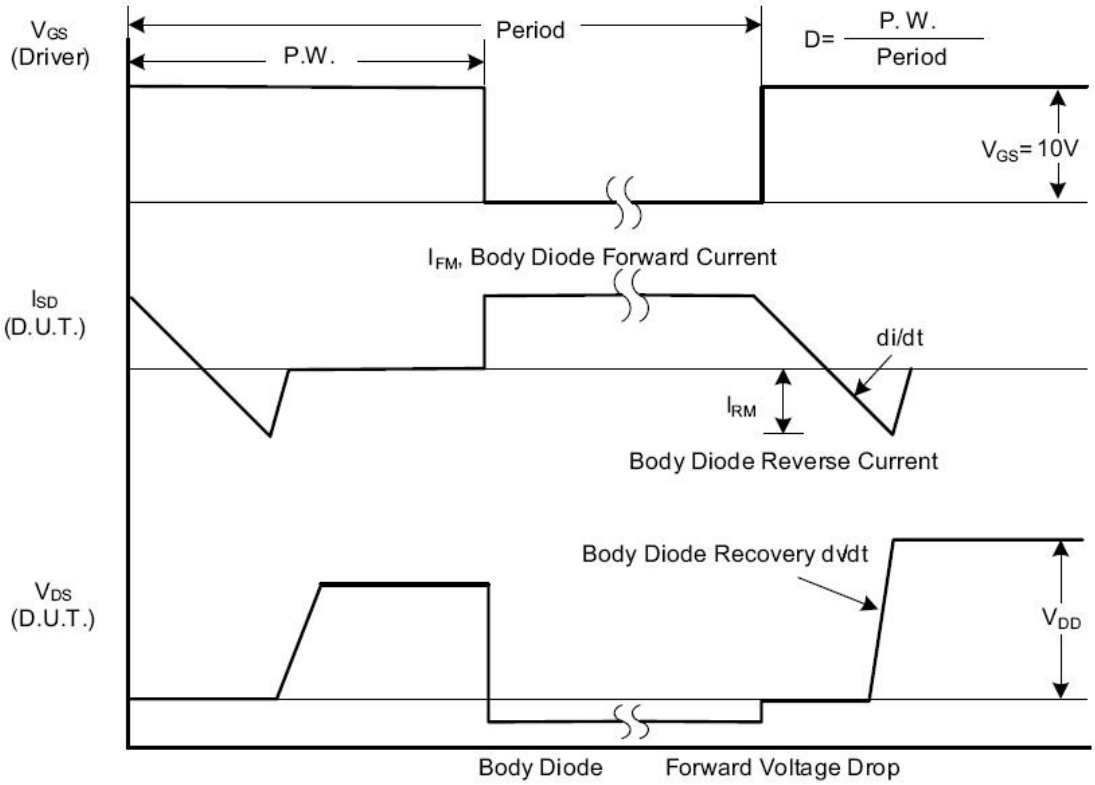


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

●Test Circuits & Waveform(cont.)

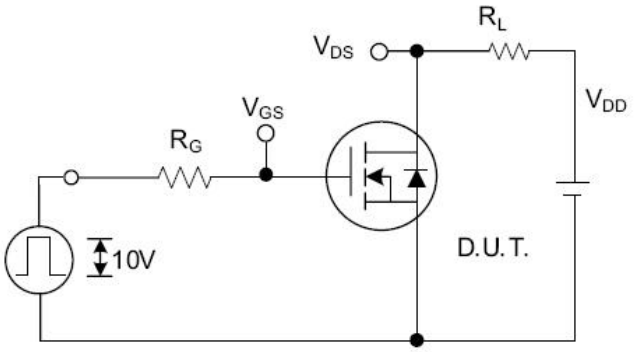


Fig. 2.1 Switching Test Circuit

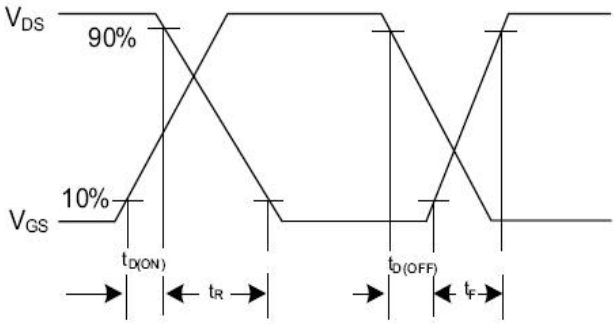


Fig. 2.2 Switching Waveforms

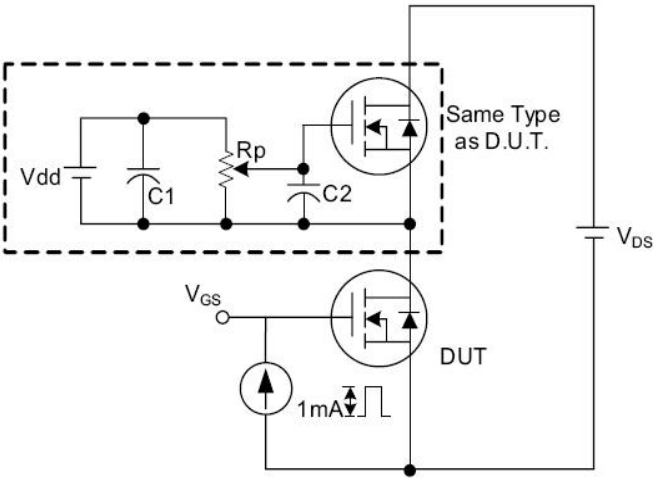


Fig. 3 . 1 Gate Charge Test Circuit

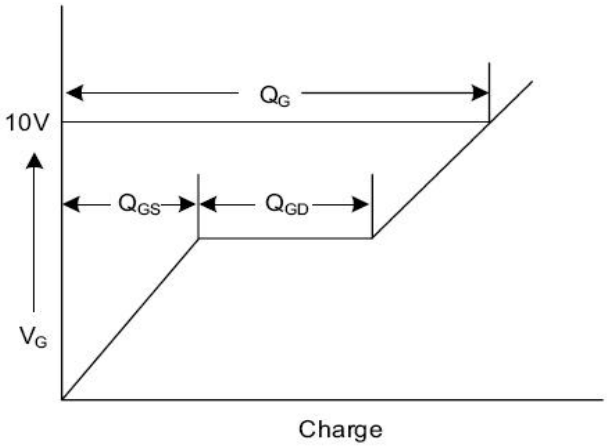


Fig. 3 . 2 Gate Charge Waveform

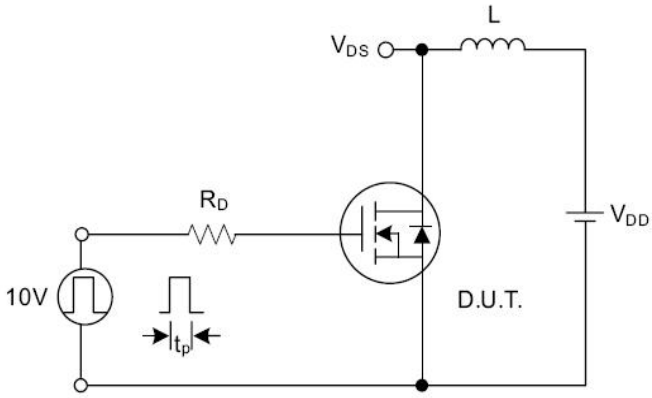


Fig. 4.1 Unclamped Inductive Switching Test Circuit

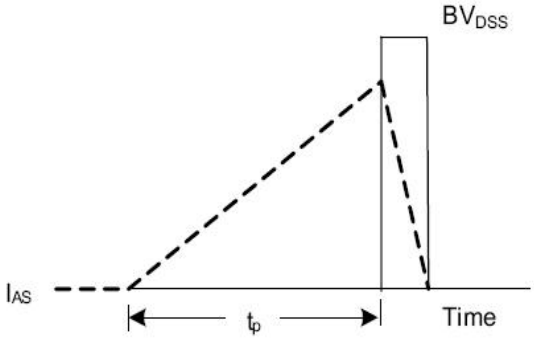


Fig. 4.2 Unclamped Inductive Switching Waveforms