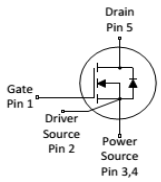
LH65R120

650V Super-Junction MOSFET

•General Description

The SJ MOSFET LH65R120 has the low $R_{DS(on)}$, low gate charge,fast switching and excellent avalanche characteristics.This device offers extremely fast and robust body diode,and is suitable for telecom and power supplies.

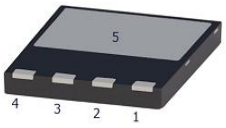


VDS =650V

$R_{DS(ON)}$ =120mΩ

ID =25A

■ RoHS COMPLIANT



DFN8*8

•Features

■Much lower Ron*A performance for On-state efficiency
■Much lower FOM for fast switching effciency

•Application

■LED/LCD/PDP TV and monitor Lighting
■Solar/Renewable/UPS-Micro Inverter System
■Power Supplies

•Ordering Information:

Part number	LH65R120
Package	DFN8*8
Basic ordering unit (pcs)	5000
Normal Package Material Ordering Code	LH65R120D8-DFN8*8-TAP
Halogen Free Ordering Code	LH65R120D8-DFN8*8-TAP-HF

•Absolute Maximum Ratings（TC =25℃）

PARAMETER		SYMBOL	Value	UNIT
Drain-Source Breakdown Voltage		BV_{DSS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	TC = 25°C	I_D	25	A
	TC = 100°C		16	
Pulsed drain current (TC = 25°C, tp limited by Tjmax)[1]		I_D pulse	60	A
Single Pulse Avalanche Energy[1]		I_{AR}	3.5	A
Single Pulse Avalanche Energy[2]		E_{AS}	484	mJ
Repetitive Avalanche Energy[1]		E_{AR}	0.7	mJ
Power Dissipation(TC=25℃)		P_D	34	W
Operating Temperature and Storage Temperature Range		T_J/T_{STG}	-55~+150	℃
MOSFET dv/dt ruggedness, V_{DS}=0…480V		dv/dt	50	V/ns
Reverse diode dv/dt, V_{DS}=0…480V,I_{SD}≤I_D		dv/dt	15	V/ns

●Electronic Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D=250uA	650	--	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=VGS,I_D=250uA	2.5	--	4.5	V
Drain-source On Resistance[3]	$R_{DS(ON)}$	V_{GS} =10V, I_D=7.5A	--	0.10	0.12	Ω
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V,T_J=25℃	--	--	1	uA
		V_{DS}=650V,V_{GS}=0V,T_J=125℃	--	--	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30	--	--	±100	nA
Forward Transconductance[3]	R_G	f=1.0MHz open drain	--	--	12	S
Input Capacitance	Ciss	V_{GS} = 0V, V_{DS} = 100V f = 1.0MHz	--	1724	--	pF
Output Capacitance	Coss		--	61	--	
Reverse transfer Capacitance	Crss		--	6	--	
Turn-on delay time	Td(on)	I_D = 25A, V_{DD} = 400V R_G = 25Ω	--	15	--	nS
Rise time	Tr		--	59	--	
Turn -Off Delay Time	Td(off)		--	121	--	
Fall time	Tf		--	44	--	
Total Gate Charge	Qg	I_D =25A, V_{DS} = 520V V_{GS} = 10V	--	38.5	---	nC
Gate-to-Source Charge	Qgs		--	8	--	
Gate-to-Drain Charge	Qgd		--	15	---	
Continuous Diode Forward Current	I_S		--	--	25	A
Pulsed Diode Forward Current	I_{SM}		--	--	60	A
Diode Forward Voltage	V_{SD}	Tj=25°C, Is=25A V_{GS} =0V	--	0.9	1.2	V
Reverse Recovery Time	trr	V_{RR}=400V, If=Is di_F/dt=100A/μs	--	423	--	ns
Reverse Recovery Charge	Qrr		--	5.3	--	uC
Peak Reverse Recovery Current	I_{RRM}		--	25	--	A

●Thermal Characteristics

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance Junction-case	Rth_{JC}	3.7	℃/W
Thermal Resistance Junction-ambient	Rth_{JA}	80	℃/W

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 1.8A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%

●Typical Characteristics T_J=25ºC,unless otherwise noted

Figure 1. Output Characteristics

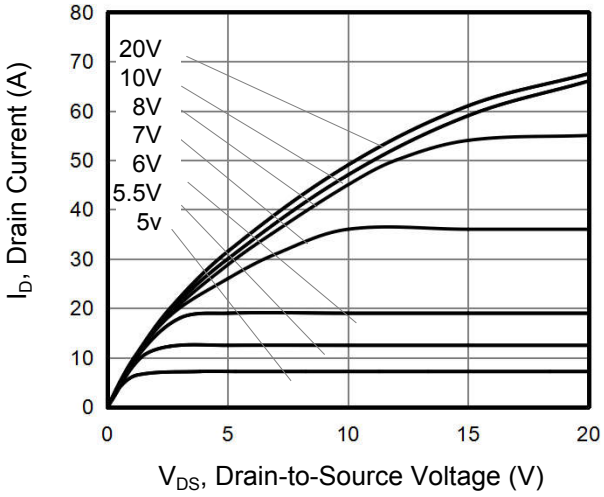


Figure 2. Transfer Characteristics

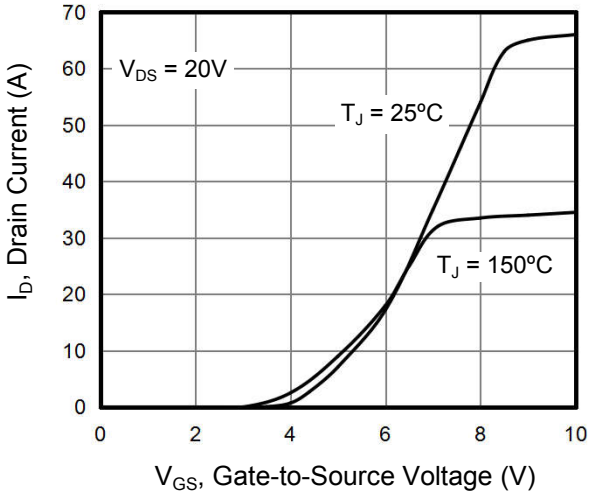


Figure 3. On-Resistance vs. Drain Current

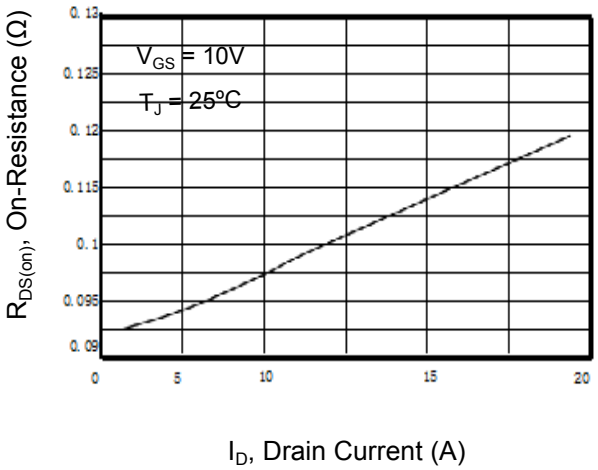


Figure 4. Capacitance

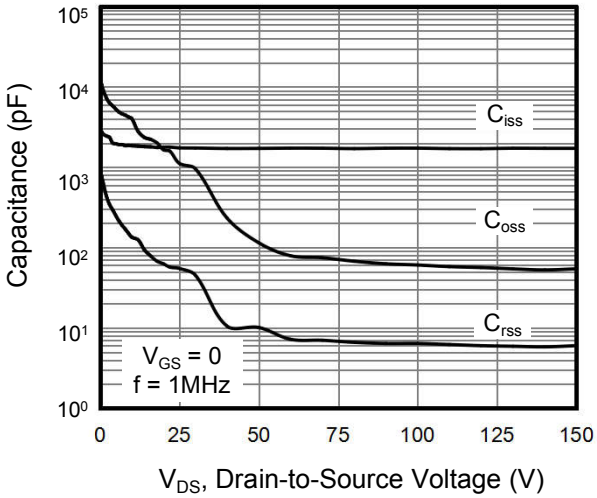


Figure 5. Gate Charge

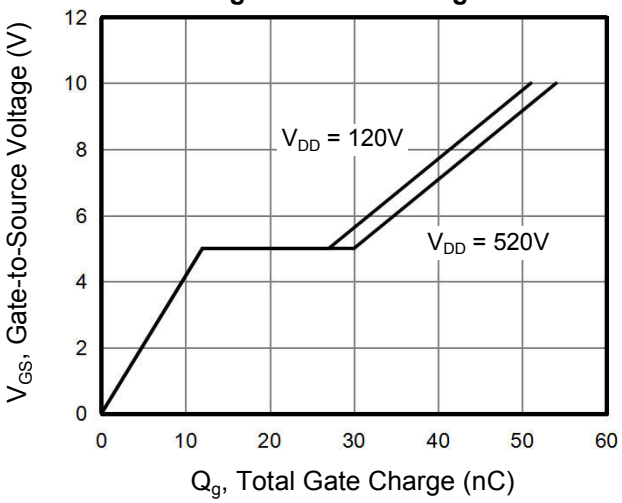
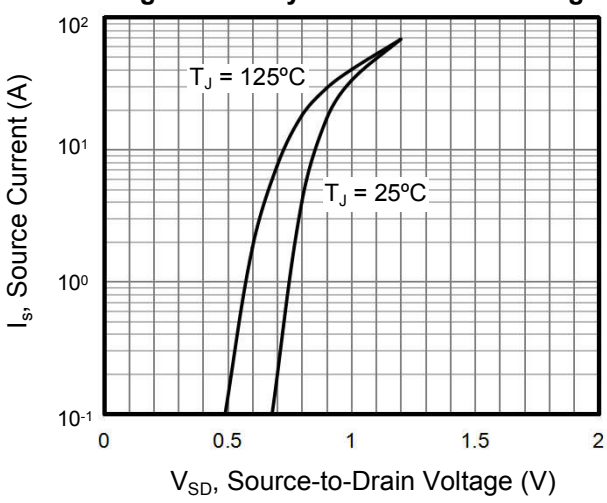


Figure 6. Body Diode Forward Voltage



●Typical Characteristics (Cont.)

Figure 7. On-Resistance vs. Junction Temperature

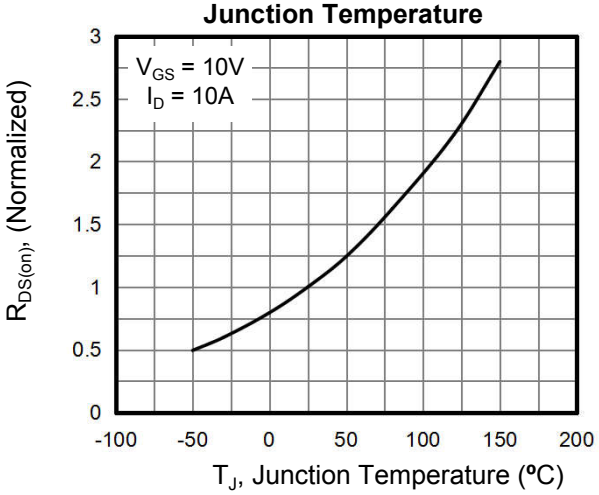


Figure 8. Threshold Voltage vs. Junction Temperature

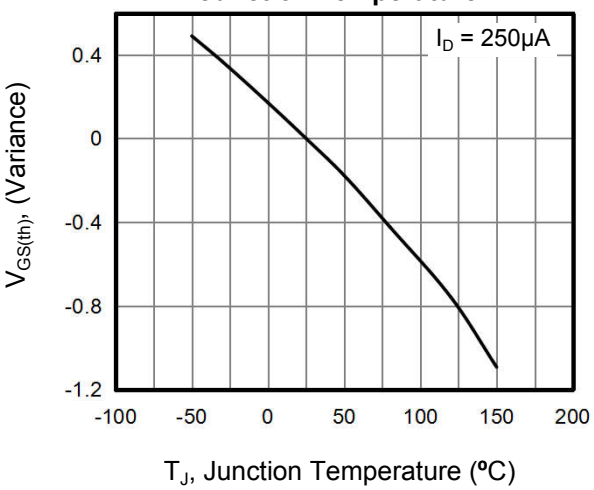


Figure 9. Safe operation area

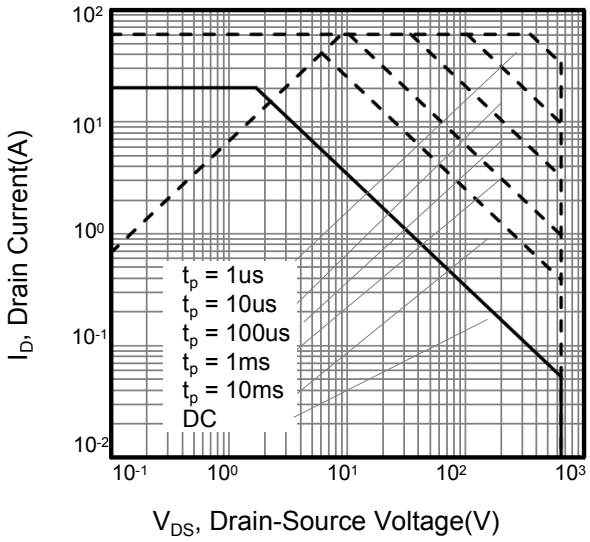
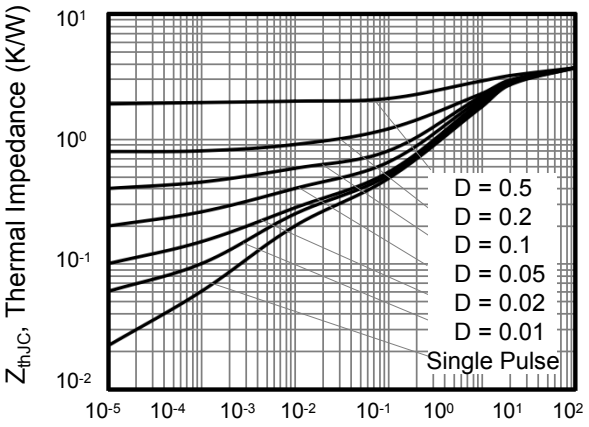


Figure 10. Transient Thermal Impedance



• Test Circuit and Waveforms

Figure A：Gate Charge Test Circuit and Waveform

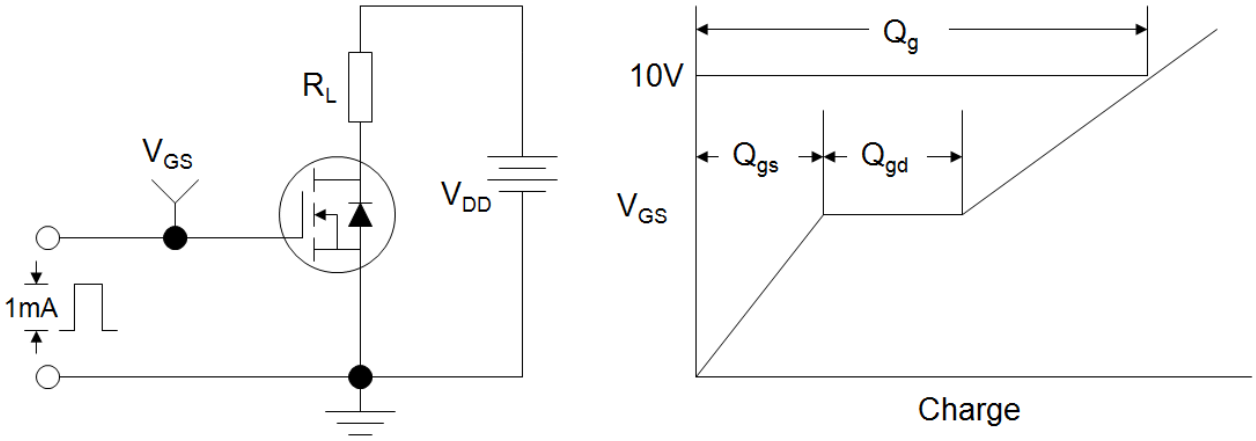


Figure B：Resistive Switching Test Circuit and Waveform

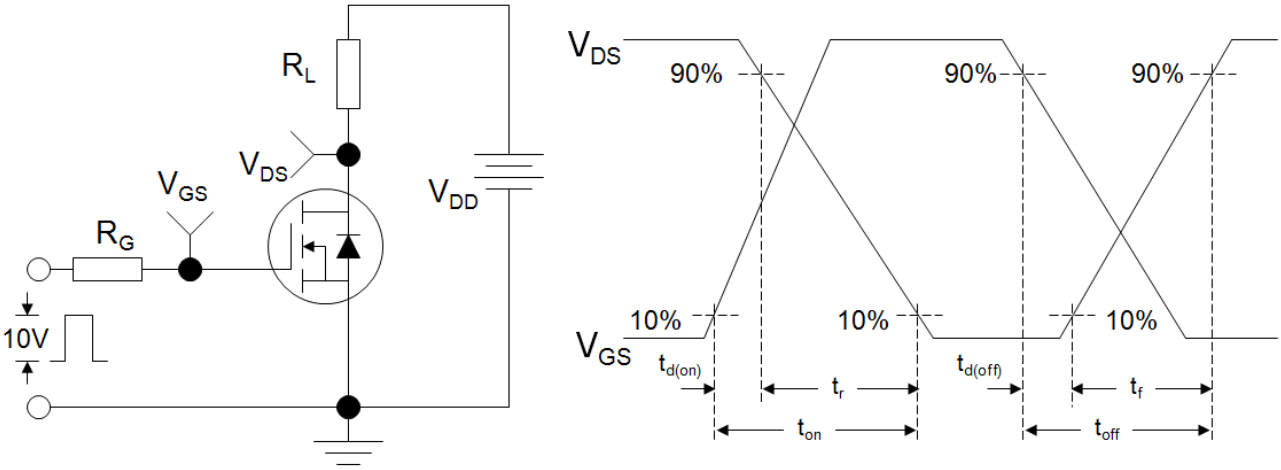
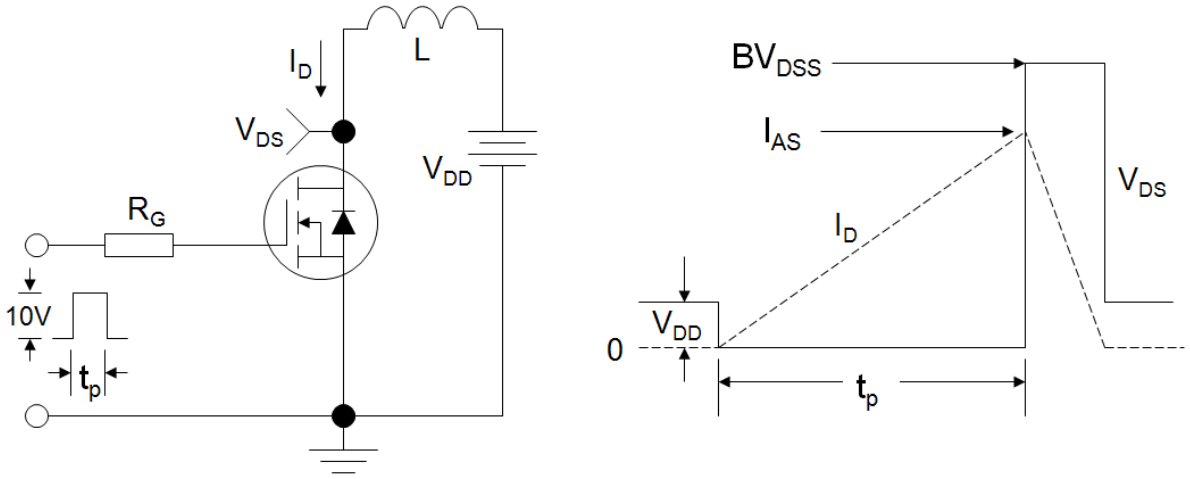


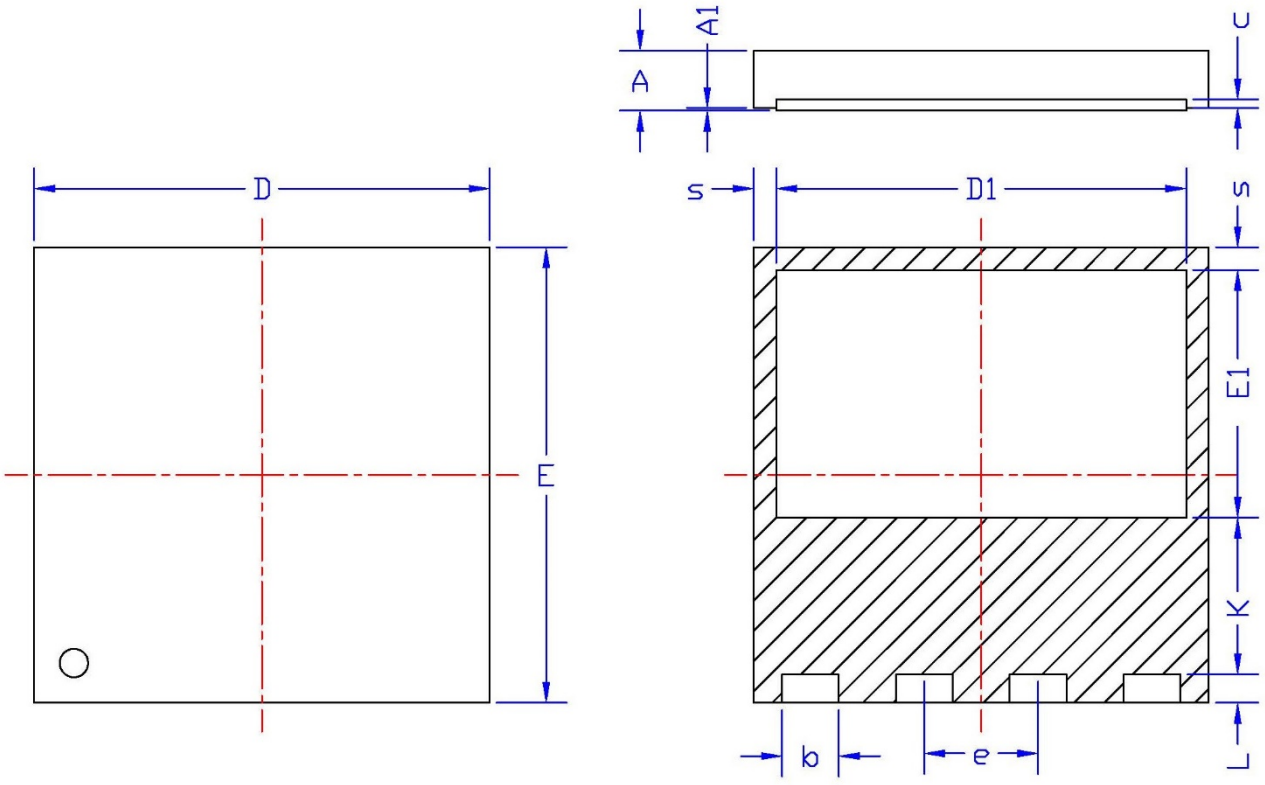
Figure C：Unclamped Inductive Switching Test Circuit and Waveform



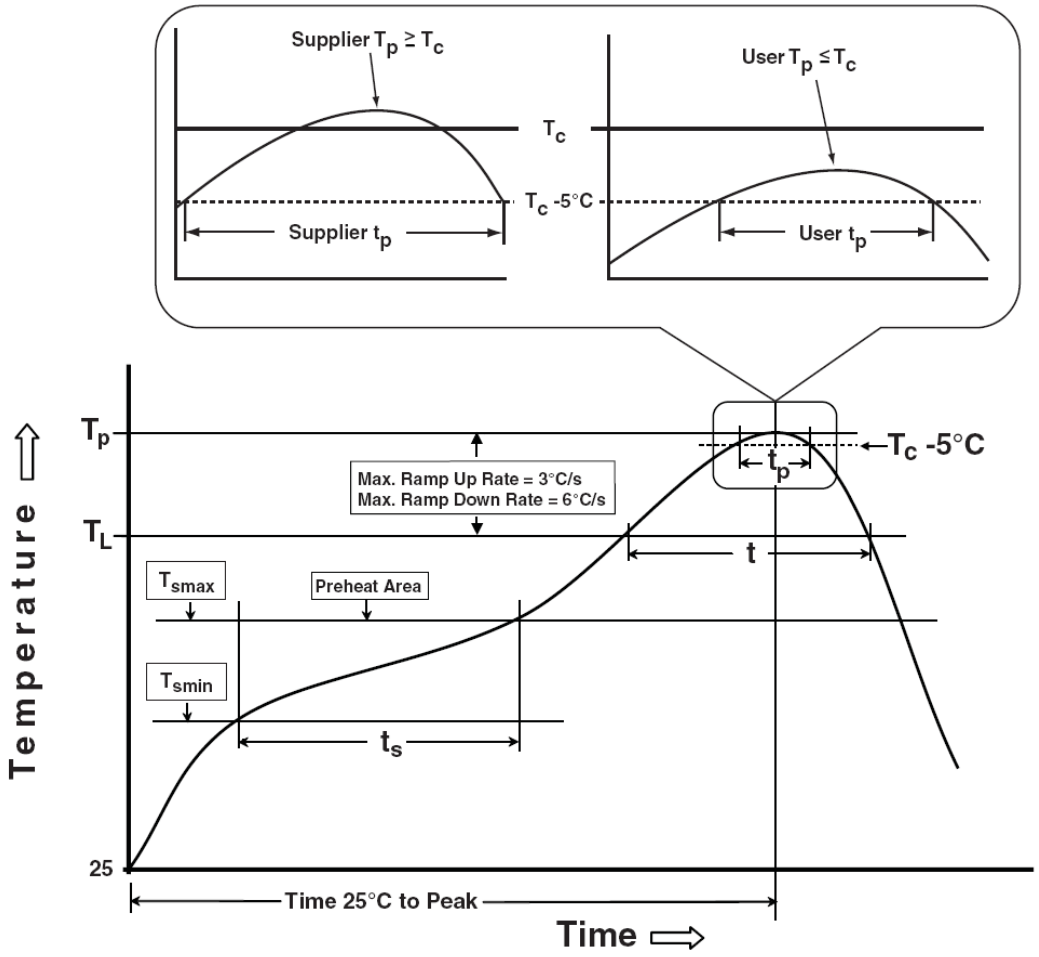
●Dimensions（DFN8*8)

Unit：mm

SYMBOL	min	max	SYMBOL	min	max
A	0.80	1.10	E1	4.20	4.50
A1	0.00	0.08	e	2.00TYP	
b	0.90	1.10	K	2.75REF	
c	0.20REF		L	1.20	2.00
D	7.85	8.15	H	0.40	0.60
D1	7.05	7.35	s	0.35	0.45
E	7.85	8.15			



- **Classification Profile**



• Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test Item	Method	Description
Solder ability	JESD-22, B012	5 SEC., 245ºC
HOLT	JESD-22, A108	1000 HRs, Bias@125ºC
PCT	JESD-22, A102	168 HRs, 100% RH, 2ATM, 121ºC
TCT	JESD-22, A104	500 Cycles, -65 ~ 150ºC